IN THE CLAIMS

Please amend the claims as follows:

1-26. (Cancelled)

27. (Currently Amended) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

an annealed metal silicide layer on the polysilicon layer;

a layer comprising $Si_xN_yO_z$:H formed over and in physical contact with the metal silicide layer, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33; the annealed metal silicide layer being the product of a process in which the metal silicide layer is subjected to an anneal treatment after the layer comprising $Si_xN_yO_z$:H is formed, wherein the layer comprising $Si_xN_yO_z$:H protects the annealed metal silicide layer during the anneal by eliminating exposure to gaseous oxygen during the anneal, further wherein a thickness of the layer comprising $Si_xN_yO_z$:H ranges between a value that is greater than about 300 Angstroms (Å) to a value of approximately 650 Å; and

a silicon nitride layer on the layer comprising $Si_xN_yO_z$:H and having a thickness greater than 1000 Å, wherein the polysilicon layer, the gate oxide layer, the metal silicide layer, the layer comprising $Si_xN_yO_z$:H, and the silicon nitride layer are patterned to form the gate stack, further wherein the layer comprising $Si_xN_yO_z$:H is configured to reduce a stress on the gate stack that is imposed by the silicon nitride layer and wherein the final thicknesses of both the silicon nitride layer and the layer comprising $Si_xN_yO_z$:H are optimized in combination to minimize reflection back into a overlying layer of photoresist.

28-35. (Cancelled)

36. (Previously Presented) The gate stack of claim 27 wherein y is from 0.02 to less than 0.1.

37. (Previously Presented) The gate stack of claim 27 wherein x = 0.5, y = 0.37 and z = 0.13.

38. (Previously Presented) The gate stack of claim 27 wherein the metal silicide layer comprises titanium.

39. - 43. (Cancelled)

44. (Currently Amended) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

an annealed, metal silicide layer on the polysilicon layer;

a means for protecting the metal silicide layer during an anneal, the means for protecting consisting of a $Si_xN_yO_z$:H layer formed over and in physical contact with the annealed, metal silicide layer, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33, the means for protecting the metal silicide layer being adapted to act as an antireflective layer, wherein the $Si_xN_yO_z$:H layer reduces a stress on the gate stack; and

a silicon nitride layer on the $Si_xN_yO_z$:H layer having a thickness greater than 1000 Å, and wherein the final thicknesses of both the silicon nitride layer and the layer comprising $Si_xN_yO_z$:H are optimized in combination to minimize reflection back into a overlying layer of photoresist.

45. (Previously Presented) The gate stack of claim 44, wherein x = 0.5, y = 0.37 and z = 0.13.

46. (Previously Presented) The gate stack of claim 44, wherein the metal silicide layer comprises titanium.

47. (Previously Presented) The gate stack of claim 44, wherein the $Si_xN_yO_z$:H layer has a thickness that ranges from a value greater than approximately 300 Å to a value of approximately 650 Å.

48. (Previously Presented) The gate stack of claim 44, wherein the means for protecting the annealed metal silicide layer is adapted to protect the metal silicide layer from gaseous oxygen during the anneal.

49. (Previously Presented) The gate stack of claim 48, wherein the means for protecting the annealed metal silicide layer is adapted to alleviate stress exerted by the silicon nitride layer on layers underlying the layer comprising $Si_xN_yO_z$:H layer.

50. (Currently Amended) A gate stack, comprising:

a gate oxide layer over a semiconductive substrate;

a polysilicon layer on the gate oxide layer;

an annealed, titanium silicide layer on the polysilicon layer;

a means for alleviating stress on underlying layers, canceling reflected radiation, and protecting the annealed, titanium silicide layer during an anneal from gaseous oxygen, the means comprising a $Si_xN_yO_z$:H layer formed over and in physical contact with the annealed, titanium silicide layer, wherein x is from 0.39 to 0.65, y is from 0.02 to 0.56, and z is from 0.05 to 0.33; and

a silicon nitride layer on the $Si_xN_yO_z$:H layer having a thickness greater than 1000 Å,and wherein the final thicknesses of both the silicon nitride layer and the layer comprising $Si_xN_yO_z$:H are optimized in combination to minimize reflection back into a overlying layer of photoresist.

51. (Previously Presented) The gate stack of claim 50, wherein x = 0.5, y = 0.37 and z = 0.13.

52. (Previously Presented) The gate stack of claim 52, wherein the $Si_xN_yO_z$:H layer has a thickness that ranges from a value greater than approximately 300 Å to a value of approximately 650 Å.